Inhibit and Synchronization

INTERPOINT® PRODUCTS APPLICATION NOTE

Although the concepts stated are universal, this application note was written specifically for Interpoint products.

INHIBIT

Applications for Inhibit

Inhibit is a feature that allows a converter to be turned on or off without cycling the input power. There are applications where this feature is desired such as keeping a converter off to conserve energy when power is not needed, sequencing the turn on of output voltages, reducing the inrush current, help prevent input impedance problems, and to delay the turn on of a converter until its input voltage is up and stable.

Delaying the turn on of a converter until its input voltage is up and stable can be important during a slow rising input voltage. During a slow rising input voltage the converter can turn on and operate at low input voltage levels. Due to the constant power demanded by the converter, operating at low input voltages creates higher input current than would otherwise occur at the nominal input voltage. Keeping the converter inhibited until the input voltage is up and stable is a way of reducing the higher current that occurs during a slow rising input voltage. Using the inhibit function also provides a means for staggering the turn on of individual converters so the inrush current does not occur during the same time interval, thus minimizing the current amplitude. Since the input impedance is proportional to the square of the input voltage, having the converters inhibited until the input voltage is up and stable can prevent input impedance problems which can occur due to low line operation that occurs with a slow rising input voltage. Staggering the turn on of converters can reduce input impedance problems further.

All Interpoint converters have a primary side inhibit function that is referenced to input common. The primary side inhibit turns the converter's pulse width modulator (PWM) off and stops switching of power components for minimal power loss. When trying to conserve battery power this can be critical as current demand from the 28 volt bus will be significantly lower when the converter is inhibited than when the load at the converter's output is not active (no load condition). The converters' datasheets provide input current specifications during inhibited conditions. A diagram of the primary inhibit circuit, that is common in many of our converters, along with a recommended inhibit interface, is shown in Figure 1. Diode D4 is present in some models and is absent in other models. The Inhibit pin is connected to the base of an NPN transistor configured as an emitter follower which provides a primary side bias to the PWM and other primary side circuitry. Pulling the Inhibit pin low will remove the primary bias which stops all power conversion. The transition of the inhibit should be fast so that the primary bias is not operating at intermediate voltages for prolonged times during the transition.

Inhibit Interfaces

As shown in Figure 1, the preferred interface for the inhibit function for most Interpoint converters is an open collector transistor, or equivalent device, that shorts the Inhibit pin to input common while the transistor is on, or leaves the Inhibit pin floating when the transistor is off. External voltages should not be applied to the Inhibit pin unless otherwise stated on the datasheet. If the datasheet states low or high voltage values for inhibit, these should not be interpreted as an external voltage that should be applied to the Inhibit pin unless it is specific. The "open inhibit pin voltage" referenced in the datasheet typically comes from the pull up resistors and Zener diode internal to the converter. The active low voltage is the maximum recommended voltage at the inhibit pin when the inhibit pin is pulled low. In order to make sure the converter is inhibited properly the open collector device should be able to pull the inhibit pin to or below the logic low value stated on the datasheet. The logic high value is the voltage that you would expect to measure at the inhibit pin if it were floating. Some converters may have a different inhibit interface but the principles are typically similar.

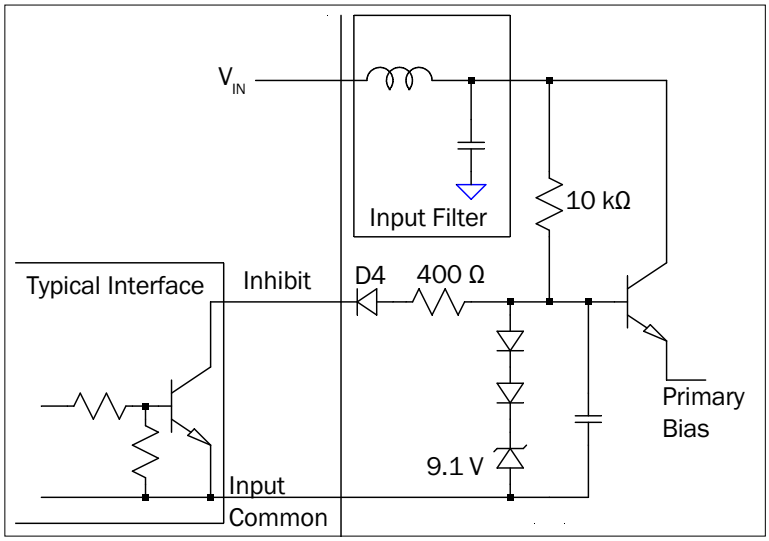

Figure 1: Typical Inhibit Interface and Primary Inhibit Circuit

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The datasheet also provides the maximum current that the Inhibit pin is capable of sourcing. In many cases the inhibit current is a function of input line voltage. This can be seen by looking at Figure 1 on page 1. When the Inhibit pin is pulled low, the current will be determined by the voltage across 400 ohm and 10 k ohm resistors in series. Since the bottom end of the 400 ohm resistor will be shorted to input common, when the interface is active, and the top of the 10 k ohm resistor is connected to V_{IN}, the current will be determined by the voltage across these series resistors. The values of the resistors may vary from model to model. Neglecting the diode, D4, which may not be present, the voltage across these resistors is the input voltage. This maximum current value is important when determining if the logic low voltage is being met. For example, many open collector comparators can sink significant current but the minimum saturated voltage while sinking 6 mA may be over 1 volt. If a converter's datasheet states a low value of 0.8 volts, and a maximum inhibit current of 8 mA, this comparator would not be a good choice. The inhibit interface should be capable of pulling the Inhibit pin to its specified logic low level while sinking the maximum current specified in the datasheet. While the inhibit interface is off it will not sink current and the interface would see the logic high voltage stated in the datasheet.

It is not recommended to connect a pull up resistor to the Inhibit pin as the converter has its own internal pull up resistor. If an external pull up resistor is desired, a diode should be added, as shown in Figure 2. This will isolate the pull up voltage from the Inhibit pin. Whenever a diode is added it will create a voltage drop which needs to be considered when meeting the converter's inhibit low specification.

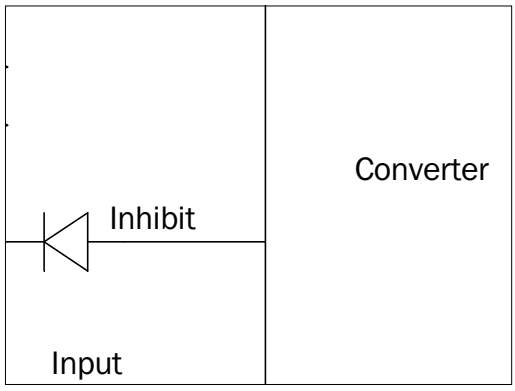

FIGURE 2: INHIBIT WITH PULL-UP RESISTOR AND DIODE

SINGLE INHIBIT INTERFACE FOR MULTIPLE CONVERTERS

In some applications it is desirable to inhibit all converters at the same time using a single control circuit. For this application all inhibit pins would need to be tied to a common inhibit interface. With many converters it is important that the inhibit pin voltage of one converter not influence the inhibit pin voltage of another converter. Preventing this would require an oring diode at the input of each inhibit pin unless the converter has an internal diode to perform this function. In Figure 1 on page 1, D4 would perform this function. In some models D4 is present which means that an external diode would not be necessary. In other models D4 is not present. If there is any uncertainty about whether there is a diode internal to the converter contact our Applications Department at powerapps@craneae.com. Figure 3 shows three converters that share a common inhibit interface with each Inhibit pin being isolated with a diode. In this case the transistor must be capable of pulling the Inhibit pin to its low level while sinking the inhibit current of three converters. The voltage drops of the oring diodes also need to be considered.

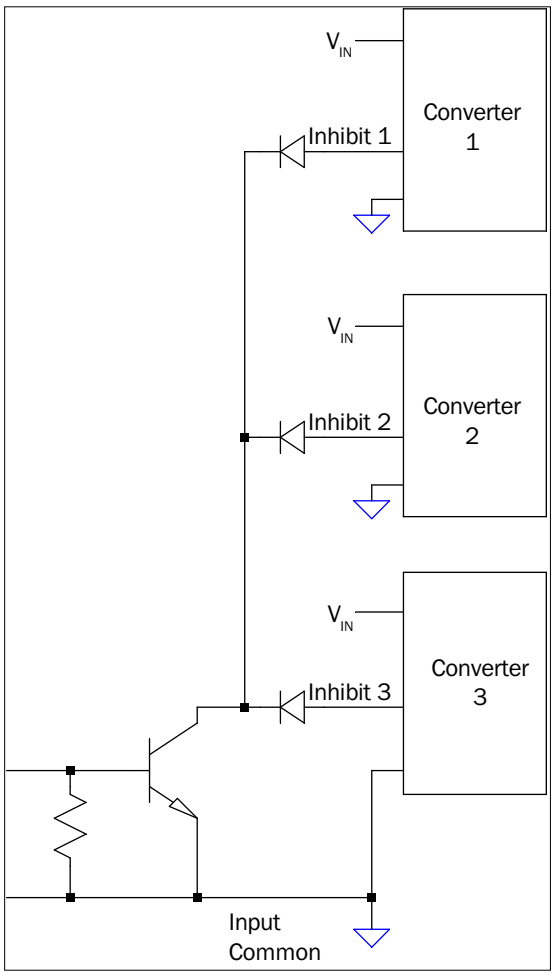

FIGURE 3: INHIBIT INTERFACE WITH MULTIPLE CONVERTERS

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INHIBIT WITH ISOLATION

In some applications, it may be necessary to reference the inhibit command to the secondary side of the power converter, which is isolated from the primary. Some of our higher power converters have a secondary side inhibit that is referenced to output common. In this case the systems inhibit interface can be an open collector transistor, or equivalent device, referenced to output common. With converters that only offer a primary side inhibit, an opto isolator can be used as to maintain isolation shown in Figure 4.

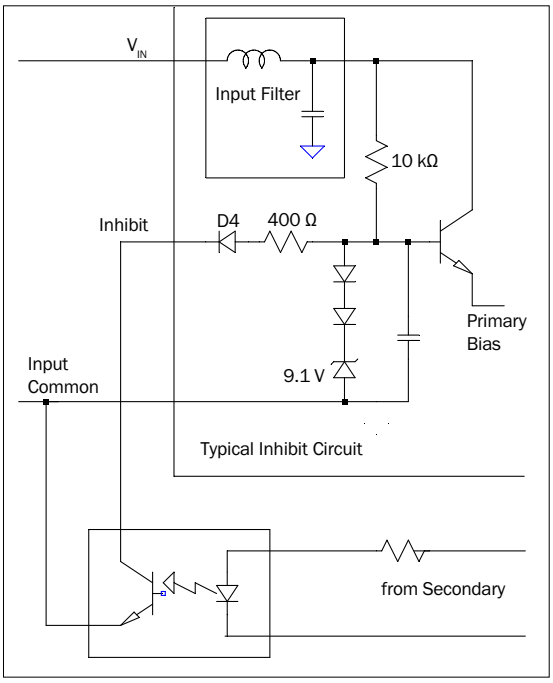

FIGURE 4: INHIBIT WITH ISOLATION

SYNCHRONIZATION

OVERVIEW

Interpoint converters have an internal clock that sets the converter's switching frequency. Most Interpoint converters have a sync input that allows the end user to adjust the converter's clock frequency within a range specified in the converter's datasheet. The sync feature allows the customer to sync the converter to desired frequency for a particular application. It can also be used where multiple converters are employed and it is desirable to have all converters running at the same frequency. An example of this would be to eliminate beat frequencies created by two or more converters running from a common input bus. The beat frequencies typically occur at a low frequency that is not attenuated by an external EMI filter. If the energy at the beat frequency is significant, and the beat frequency lies within the EMI specification's lower frequency band, it is possible that the system may not meet the EMI specification. Beat frequencies are typically below 50 kHz where the EMI limits are much more lenient at these lower frequencies. Beat frequencies are typically not a problem in most applications.

SYNC IN INTERPOINT CONVERTERS

The sync/clock circuit for the MFL converter is shown in Figure 5. Figure 5 is also representative of the sync circuit for the MHF+ singles and duals (not triples), MTR, FMTR and other (but not all) Interpoint converters, with the exception that the "sync out" function is absent for these converters. Of the converters listed here the MFL is the only converter that has a "sync out" function.

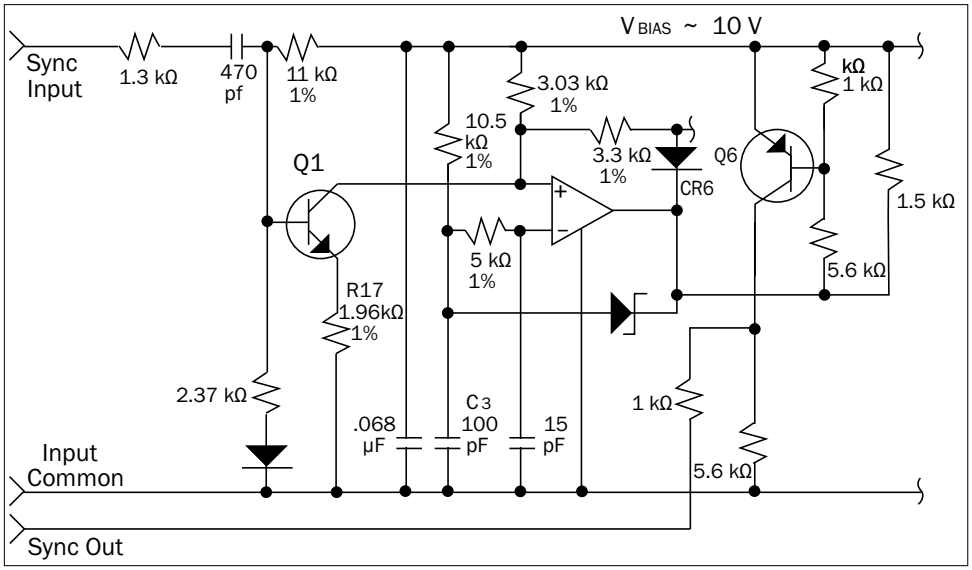

FIGURE 5: TYPICAL INTERPOINT SYNC CLOCK CIRCUIT

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Ideal Sync Pulse

The ideal sync input for the circuit of Figure 5 on page 3 is a 0 to 5 volt, 40%-60% duty cycle square wave with rise and fall times of less than 150 nanoseconds. What is important for the circuit is the peak to peak value of the sync signal versus the minimum and maximum values. Having a sync signal of 0 to 5 volts or -2.5 to +2.5 volts would provide the same results because the sync signal is an AC coupled signal. Refer to the converter's datasheet for the recommended amplitude and duty cycles for the particular model. An interface driver with Z_{OUT} of less than 50 Ω is recommended. If unsure about the type of sync circuit internal to an Interpoint converter contact powerapps@craneae.com.

Sync Out - MFL

The MFL also has a sync out function with a pulse that transitions from around 0 volts to a little over 10 volts unloaded. The sync out duty cycle is typically around 22% with a fast rise and slower decay. The sync out function of the MFL can be used to drive the sync in of another MFL converter allowing both converters to run at the same frequency. The sync in specification for the MFL is close to 5 volts peak-to-peak and the unloaded Sync Out pin is close to 10 volts peak-to-peak. However, when connecting sync out of one MFL to sync in of another MFL the loading effect will drop the voltage close to the sync in specification of 5 volts peak-to-peak. Many MFL style converters can be daisy chained together in this manner so that they all run at the same frequency. This would be good when powering multiple converters from a single EMI filter or running MFL converters in parallel operation. In addition, the sync out of an MFL can also be used to sync other converters that share the sync circuitry shown in Figure 5 on page 3 if the free running frequency of the MFL is within the "sync in" range of the converter it is syncing. The free running frequencies and the allowable sync range can be found on the converter's datasheet.

Application of a Sync Signal

With some converters the application of sync may cause a slight voltage transient on the converter's output if the converter is running during the application of sync. An alternative method of applying sync would be to have the converter inhibited, apply the sync signal, then release the inhibit allowing the converter to turn on with the sync already applied. This would eliminate the possibility of output voltage transients that may occur during the application of sync. If using the sync function, it is important to always stay within the frequency range specified in the datasheet as the converter may run too hot or be damaged if operating outside of these limits. In some applications when an external sync is first applied the system sync signal may be at some undesirable frequency or amplitude until the system clock signal has stabilized. If this is a possibility, having the converter inhibited until the external sync signal has stabilized will ensure that the instability will not be seen by the converter.

Isolating the Sync Circuit

The sync input of most devices is referenced to input common. In applications where the system clock is referenced to output common of the converter, or a ground other than the converter's input common, an isolated interface would be required. An isolated interface usually involves a pulse transformer as shown in Figure 6. Here a low impedance complementary output buffer drives a pulse transformer. A capacitor in series with the primary of the pulse transformer removes the DC and helps prevent the pulse transformer from saturating. If the pulse transformer is driven directly, without the series capacitor, care must be taken to ensure that the core of the pulse transformer is reset to zero on a cycle by cycle basis to avoid core saturation. The low impedance buffer allows multiple power converters to be driven in parallel. Modeling, and bread boarding your drive circuit is highly recommended as some bipolar, totem pole drivers, provide a distorted signal. To minimize unwanted leakage inductance, bifilar winding the pulse transformer is recommended.

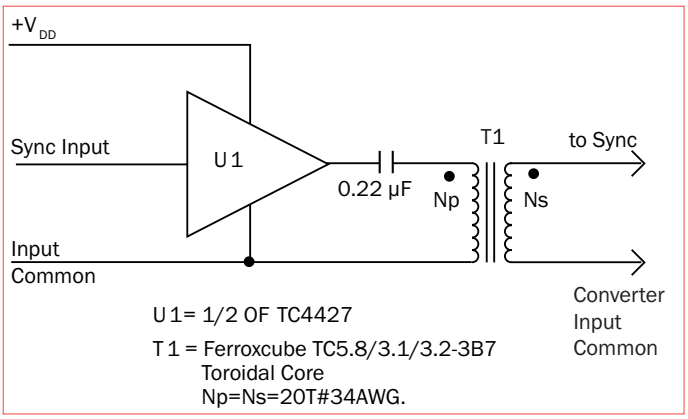

Figure 6: Isolated Sync Interface

Layout

Sync signals can have fast transitioning edges that can radiate noise and couple to other circuitry. Overlapping sync traces with their return trace is a good design practice. This will help provide a cleaner signal and reduced radiated and conducted noise. Where multiple converters are used with their inputs paralleled, and sync input connected to a common pulse driver, care must be taken to ensure that unwanted noise signals, due to ground loops, do not appear as unwanted sync inputs. When a sync terminal is referenced to the power converter's input common, any noise between this return and the sync driver's return will appear as a spurious sync input. This can cause jitter and low frequency components in the input and output spectral noise. In this case eliminate any ground loops or use a pulse transformer to decouple the noise. Use pulse transformers with one or more isolated outputs as required.

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Figure 7 shows an example where three converter inputs are paralleled and synchronized from the same driver. The sync input of converter #1 is driven directly from the sync pulse driver because its input common is close to the converter #1 input common. Power converters #2 and #3 share a common ground loop between their input commons and the driver's input common. A dual secondary pulse transformer is used to decouple the sync terminals from noise in the ground loop.

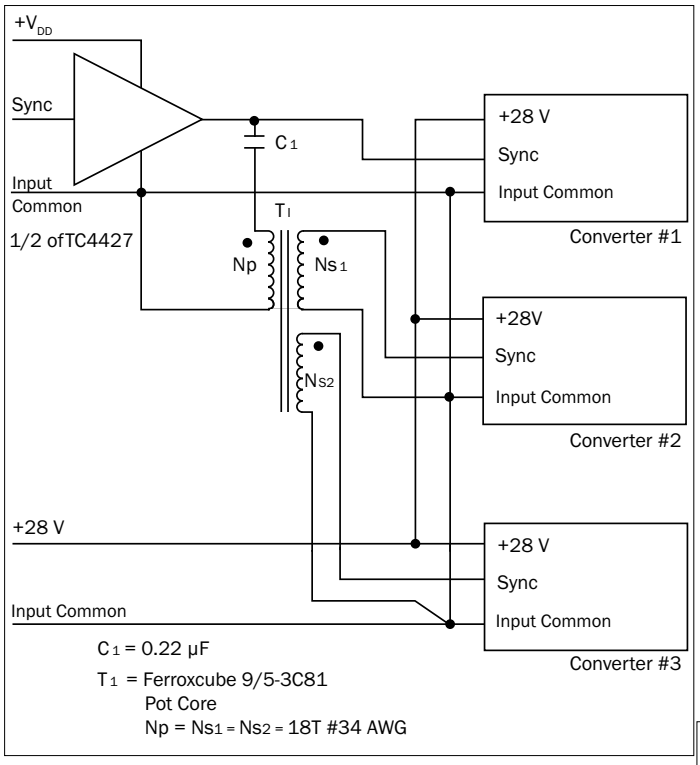

FIGURE 7: SYNC CIRCUIT APPLICATION

INHIBIT AND SYNCHRONIZATION WHEN USING AN EMI FILTER

When switching power supplies are used with external EMI filters, extra care must be exercised in locating the external ground returns for the inhibit and/or synchronization drivers. Referencing these ground returns to anything other than the power converter's 28 volt input common pin may cause damage to the power converter. The external EMI filters usually incorporate a balun as part of the common mode noise filter (refer to Figure 8). One winding of the balun is in series with the filter input common line. If the return for the sync generator or the inhibit pull down switch is terminated at the input side of the filter any noise developed across this balun winding will appear as an input in series with either of these functions. The voltage developed across this winding will consist of high frequency noise components with a peak-to-peak amplitude of several volts. This is sufficient to disrupt the converter's PWM, resulting in possible saturation of the converter's main power transformer possibly causing damage to the power train components. The impedance of the balun's return winding can also significantly distort the shape of the sync signal due to its high impedance at the sync frequency.

Figure 8 is an example where two power converters are connected to a common external EMI filter and both the inhibit and sync functions are in use. A pulse transformer isolates the sync input from the ground loop containing the balun internal to the EMI filter. Without isolation, voltage across the balun's return line winding would be in series with the sync generator. The inhibit function is controlled by a transistor is referenced to input common of the power converters. It is assumed that the power converters are located next to each other so that any effective series resistance, or series inductance, associated with the common ground between the two converters is negligible. Isolation diodes are used to allow the inhibit terminals to be controlled from a single source. Some models may not need these diodes if they have an isolating diode as part of their internal circuitry. Check the datasheet's block diagram if it exists, or contact the Applications Department at powerapps@craneae.com to see if a diode is needed when configured to inhibit multiple converters. The Applications Department will be able to help with any other questions and ensure a good design.

If the sync or inhibit function are not going to be used it is important to check the datasheet for the recommended connections of un-used pins.

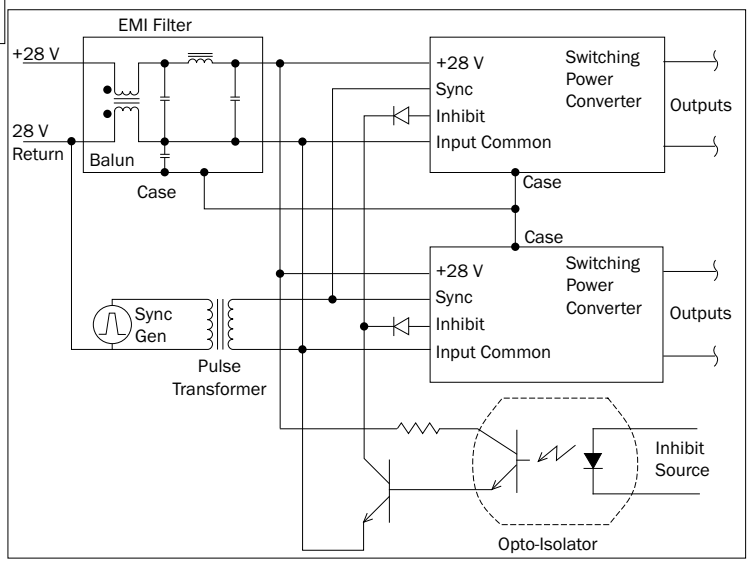

FIGURE 8: TWO CONVERTERS CONNECTED TO A COMMON FILTER