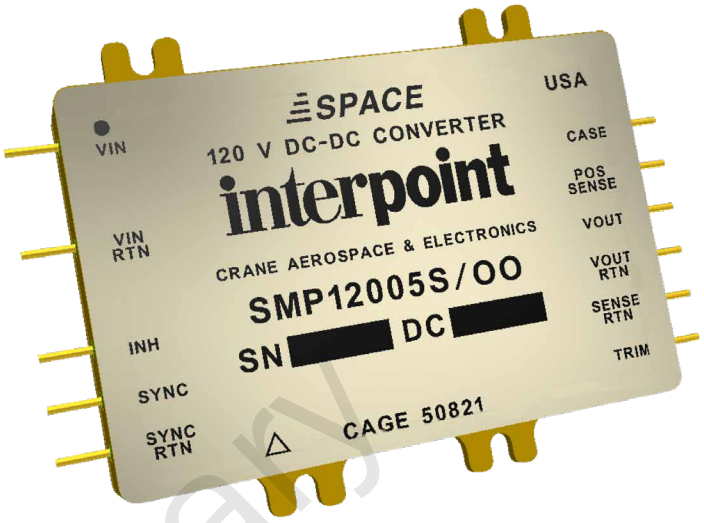
SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

FEATURES

- Radiation tolerant space converter [1]
  - Single event effects (SEE) LET performance to 43 MeV cm^2/mg
  - Total ionizing dose (TID) guaranteed per MIL-STD-883 method 1019, radiation hardness assurance (RHA) P=30 krad, L=50 krad, R = 100 krad
  - 50 - 300 rad(Si)/sec dose rate (Condition A)
  - 10 mrad(Si)/sec dose rate (Condition D)
- Output overvoltage protection
- Inrush current limit
- Output trim from ±10% of nominal
- Operating temperature -55° to +125°C
- Screened to MIL-PRF-38534 Class H and K [1]
- Input voltage range 80-160 volts
- Transient protection 180 volts for 100 ms
- Fully isolated, magnetic feedback
- Fixed high frequency switching
- Remote sense
- Inhibit function
- Synchronization input
- Indefinite short circuit protection



MODELS OUTPUT VOLTAGE (V)
SINGLE
5
28

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HIGH VOLTAGE WARNING

Care should be taken when the converter is in a live circuit.
There is the potential for up to 180 volts at the input power pins.

DESCRIPTION

The Interpoint® SMP120 Series™ of DC-DC converters offers up to 49 watts of power in a radiation tolerant design. The low profile SMP120 converters are manufactured in our fully certified and qualified MIL-PRF-38534 Class K production facility and packaged in hermetically sealed steel cases. They are ideal for use in programs requiring high reliability, small size, and high levels of radiation hardness assurance.

The SMP120 converters are switching regulators which use a current mode control single switch forward design with a nominal switching frequency of 500 kHz. Close regulation is maintained with advanced constant frequency pulse width modulation design techniques. The SMP120's current mode control topology provides high levels of input-to-output ripple rejection.

RADIATION TOLERANCE

The SMP120 DC-DC converters are designed to provide continuous normal operation through radiation levels associated with space missions and in tactical and strategic military environments. The RHA level converters will meet their SMD electrical characteristics up to the rated TID levels at both low dose rates (condition D method 1019 of MIL-STD-883) and high does rates (condition A of method 1019 of MIL-STD-883).

These levels of radiation tolerance make the SMP120 converters suitable to provide power to electronic systems in programs where operation in high radiation environments is required.

1. Screened to MIL-PRF-38534. Class H and K and RHA levels are pending product validation.

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Screening

SMP120 converters offer screening options of space prototype (0), Class H or K and radiation hardness assurance (RHA) levels P 30 krad(Si), L 50 krad(Si) or R 100 krad(Si). The converters are screened to MIL-PRF-38534. Class H and K and RHA levels are pending product validation.

Radiation performance,

- SEE LET performance 43 MeV cm^2/mg
- SEB (no burn-out) 43 MeV cm^2/mg
- SEL (no latch-up) 43 MeV cm^2/mg
- SET 43 MeV cm^2/mg

Undervoltage Lockout

The SMP120 converters have an undervoltage lockout (UVLO) circuit that will hold the converter off until the input voltage rises to approximately 75 volts at which point power conversion will begin. When the input voltage falls to approximately 69 volts, the converter will power off. When the input voltage is between 69 and 75 volts, the output voltage may not meet nominal voltage regulation specifications.

Output Overvoltage protection

The SMP120 overvoltage protection circuit comprises a redundant reference voltage and comparator to detect when the output voltage exceeds approximately 130% of the nominal output voltage. When an output overvoltage condition is detected, the protection circuit forces the converter to shutdown for a few milliseconds and initiate a restart. If the overvoltage condition persists, the protection circuit will repeat the shutdown/restart cycle until the overvoltage condition goes away or the converter is inhibited externally.

When using the trim function, the margin between the trimmed voltage and the overvoltage threshold will be reduced since the overvoltage threshold is fixed at approximately 130% of the nominal output voltage.

Inrush Current Limiter

The SMP120 inrush current limiter comprises an N-Channel MOSFET as a simple timer. When the inhibit pin is released, a high voltage current source charges a capacitor that is connected between the gate and source of the current limiter FET. This causes the gate voltage to rise at a rate determined by the current and capacitor. When the gate voltage approaches the FET threshold voltage, the FET starts to conduct. Initially, the FET appears as a large resistance in series with the internal capacitance of the converter allowing the capacitance to charge slowly and limiting the inrush current at start up. As the gate voltage increases, the resistance of the current limiter FET decreases until the FET is fully on thereby minimizing the power loss due to the current limit circuit.

Sense on 5 Volt Single Output

Tight load regulation is maintained via a wide bandwidth magnetic feedback and through the use of remote sense on the 5 volt single output models. The sense pin function allows a remote connection for the voltage regulation circuit to compensate for voltage drops between the converter and the point of use. Up to 500 mV is allowed between the positive sense and the positive output and between the sense return and output return.

Note that if the sense pins are connected but the output voltage pins are not, the converter may be damaged.

CAUTION: The converter will be permanently damaged if the positive sense (pin 10) is shorted to ground (pins 7 or 8), or if the sense return is connected to the positive output (pins 9 or 10). Damage may also result if the output common or positive output is disconnected from the load when the remote sense leads are connected to the load.

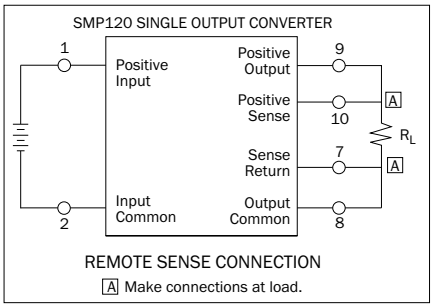

Figure 1: Remote Sense

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Inhibit

The SMP120 Series incorporates an inhibit terminal that can be used to disable internal switching. It is not recommended to tie the Inhibit pin of an SMP120 directly to the Inhibit pin of another converter as the SMP120 Inhibit pin can sink current.

When pulling multiple inhibit signals low, a separate interface is recommended for each SMP120. The converter is inhibited when the Inhibit pin is pulled low (<1.0 V). In the inhibit mode the inhibit pin current requirement is less than ~500 µA. The converter resumes normal operation when an open circuit is applied to the Inhibit pin or the Inhibit pin is released. The open circuit voltage of the Inhibit pin is 10 to 13.6 volts.

To enable the converter use an open collector on the Inhibit pin or leave it unconnected. See Figure 2.

Following a shutdown event by assertion of the inhibit function the assert to de-assert delay time must be at least 10 ms for no capacitive loading and 40 ms for maximum capacitive loading. It is highly recommended that a debounce circuit be used to drive the inhibit signal to prevent rapid turn-off and turn-on as this may cause damage to the converter.

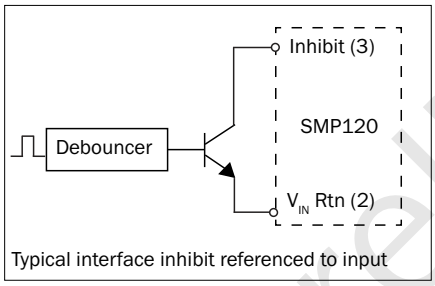

FIGURE 2: INHIBIT INTERFACE (DELAY NOT ADDED)

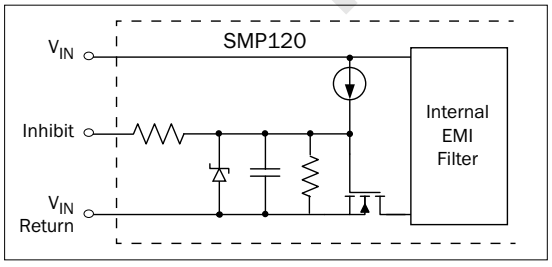

FIGURE 3: INHIBIT

Operation

The SMP120 is a single-ended current mode control forward converter. Rectification is performed using Schottky diodes.

Output Power De-rating

The output power of the SMP120 must be derated to 34 watts when operated on at a baseplate temperature of 125°C. The derating for the 28 volt model starts at 85°C and 110°C for the 5 volt model. The de-rating is linear between the starting temperature to 125°C.

Extended operation of the converter in an overload condition with a baseplate temperature of 85°C, for the 28 volt single and 110°C for the 5 volt single may result in permanent damage to the converter. Operation in an overload condition at 85°C or above is permissible for up to 10 minutes.

Effects of External Voltage Source and Remote Sense Connections

Care must be taken to avoid accidental disconnection of the Positive Output (Pin 10) or Output Common (Pin 8) when Remote Sense is used. If the sense pins are connected to the load, but the output power pins are not connected to the load, then the converter may be damaged. Also, care should be taken not to swap the sense pin connections as permanent damage to the unit will result.

Load Current Sharing

The SMP120 converters do not support load current sharing or parallel operation.

Powering Constant Current Loads

The SMP120 uses foldback current limiting to minimize the internal power dissipation in the event of a short circuit at the output of the converter. The foldback current limit circuit reduces the current limit threshold to approximately 50% of the room temperature full load current when the output voltage under overload falls below 2 volts. The output voltage of the SMP120 may not reach regulation if a pure constant current 100% load is applied during startup. Most loads generally have a combination of resistive, capacitive, and constant current behavior. Constant current loads are typically only seen in test laboratory environments.

To ensure that the SMP120 will start properly with a pure constant current load, the loading should be less than 50% of the full load current. The constant current load may then be increased to 100% once the SMP120 output voltage has reached it specified value.

When powering a 100% mixed load, the constant current portion should be less than 50% with the balance being resistive.

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SEQUENCING

The SMP120 converters are well suited for providing an intermediate bus voltage to power low voltage DC-DC converters and Point of Load (POL) converters. In order to ensure predictable start up and turn off behavior, proper sequencing of the SMP120 and associated load is highly recommended. The timing diagram, Figure 4, shows a typical sequence of the application/removal of power and enabling/inhibiting of the SMP120 and load.

Ideally, the SMP120 is enabled after the input power has stabilized. Once the SMP120 output voltage has stabilized, the POL may be enabled. During turn off, the sequence is reversed with one exception, the SMP120 and POL may be inhibited simultaneously, then the input power may be removed. Adhering to this sequencing protocol will ensure that the SMP120 and POL will power up and down in a predictable manner.

Table 1 below describes the timing in more detail.

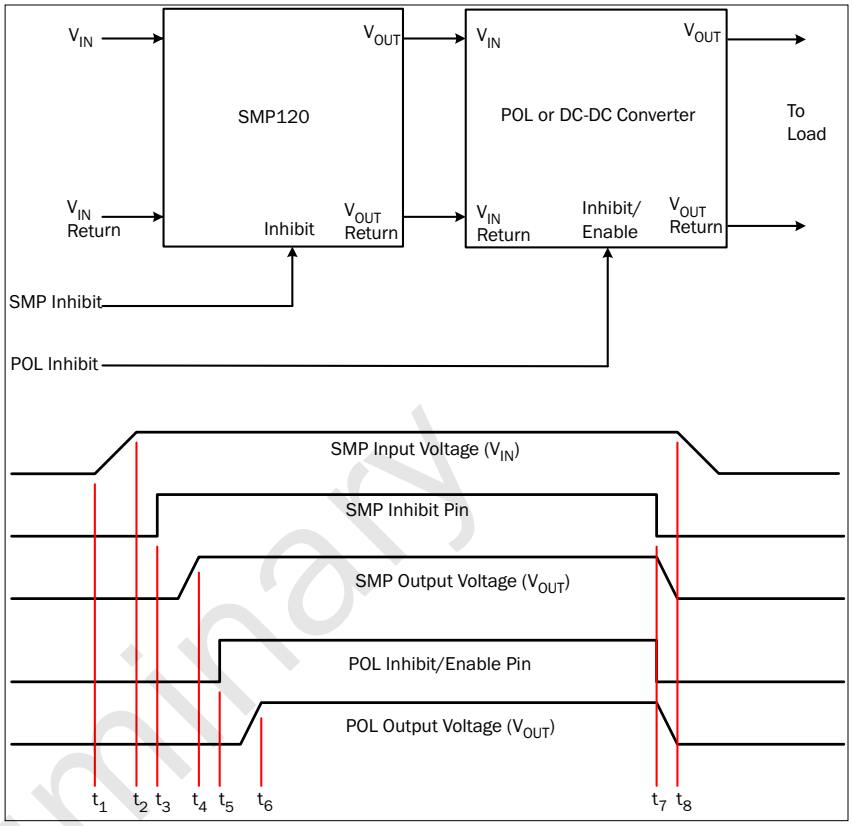

FIGURE 4: SEQUENCE DIAGRAM

Sequence	Description	Time
t1 – t2	Initial application of power	Dependent on system characteristics
t2 – t3	Input power stabilization	Dependent on system characteristics
t3	Enable SMP120	
t3 - t4	SMP120 Output Voltage start up	25 ms max
t4 – t5	SMP120 Output Voltage stabilization time	<1 ms
t5	Enable POL	
t5 – t6	POL Output Voltage start up	Dependent on POL
t6 – t7	Normal operation	
t7	Inhibit SMP120 and POL, may be simultaneous	
t7 – t8	SMP120 and POL output voltage turn off and decay	Dependent on load
t8	Removal of input power.	

TABLE 1: SEQUENCE TIMING

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SMP120 Single Output Space DC-DC Converters

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SYNCHRONIZATION

The Sync Input pin is isolated which allows the Sync Return pin to be tied to the primary side, secondary side, or float with respect to all inputs and outputs. The sync function can only increase the switching frequency above the converter's free running frequency.

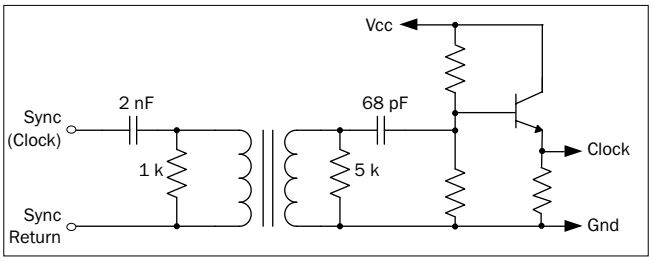

FIGURE 5: SYNC

EMI

The SMP120 includes an integrated 2-section, damped LC EMI filter to reduce the reflected input current ripple. The filter is damped to reduce the peaking at resonance to minimize the stress on the EMI filter and power components. The damping also serves to minimize the interaction of the filter output impedance with the negative input impedance of the DC-DC converter. The filter does not reduce conducted emissions to MIL-STD 461 levels.

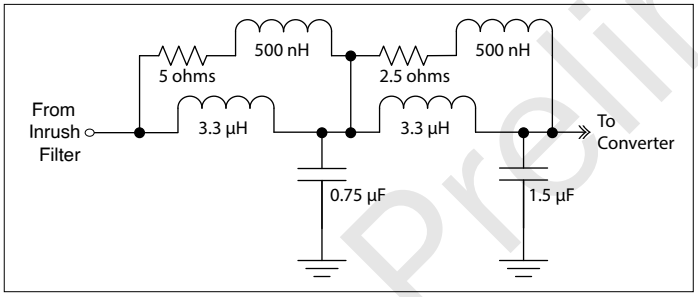

FIGURE 6: BUILT IN EMI FILTER

ELECTROSTATIC DISCHARGE SENSITIVITY (ESD)

The SMP120 Series converters ESD rating is TBD.

OUTPUT VOLTAGE TRIM

The output voltage may be trimmed up or down approximately +/-10% by tying the Trim pin to ground or tied to V_{OUT} pin via a programming resistor (R_T).

To trim up connect the trim resistor to V_{OUT} Return (pin 8). For the 5 volt singles, Sense Return (pin 7) must also be connected to V_{OUT} Return (pin 8).

To trim down connect the trim resistor to V_{OUT} (pin 9). For the 5 volt singles, Positive Sense (pin 10) must also be connected to V_{OUT} (pin 9).

R_T is the external trim resistor in kilo ohms.

X = V_{OUT} -2.5 (where V_{OUT} is the desired output voltage)

5 volt output trim
Trim up: R_T = (12.475/(X-2.5))-16.5.
Trim down; R_T = (4.99*X/(2.5-X))-16.5.

28 volt output trim
Trim up: R_T = (127.75/(X-25.6012))-33.2
Trim down: R_T = (51.1*X/(25.6012-X))- 33.2

NOTE: Do not exceed maximum output current rating when trimming down.

NOTE: Do not exceed maximum output power rating when trimming up.

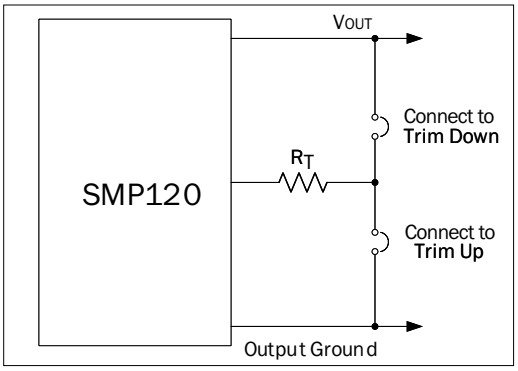

FIGURE 7: TRIM

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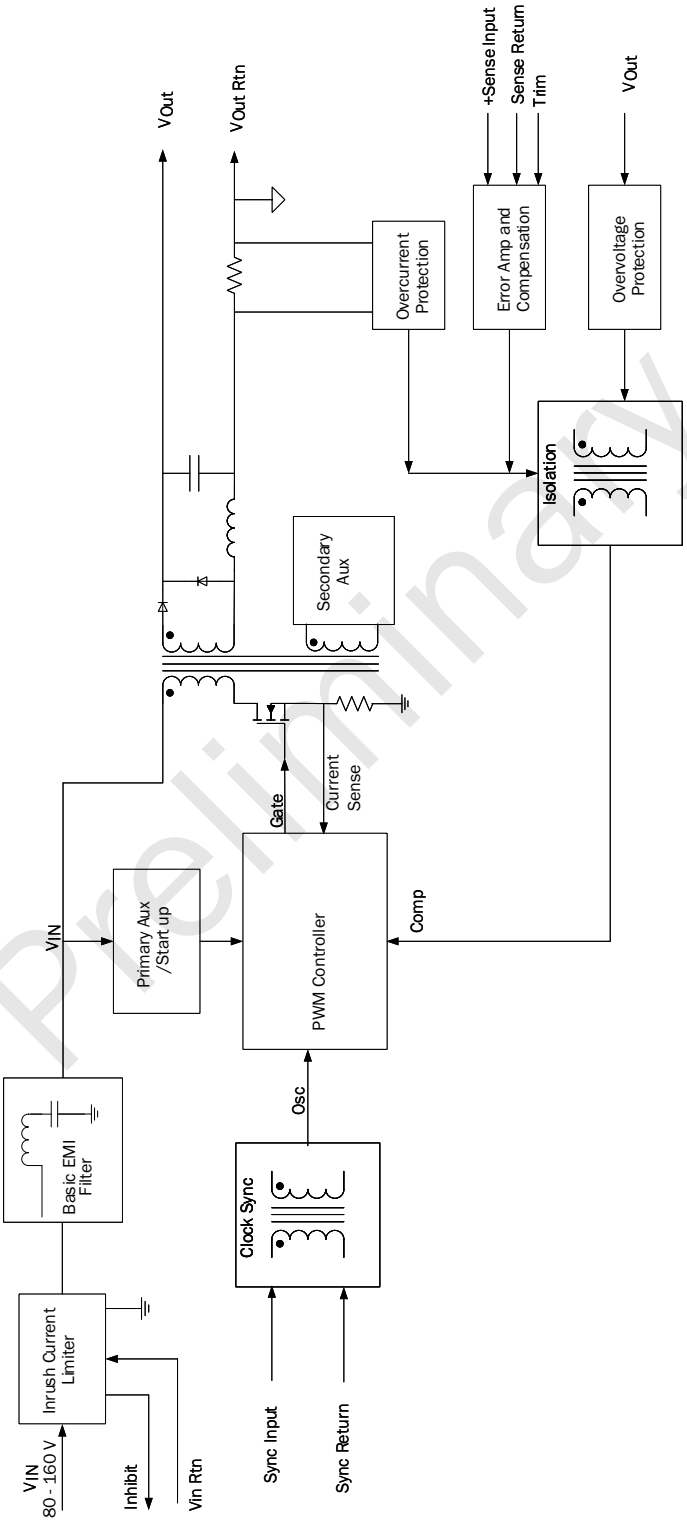

FIGURE 8: SMP120 BLOCK DIAGRAM 5 VOLT SINGLE

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SMP120 Single Output Space DC-DC Converters

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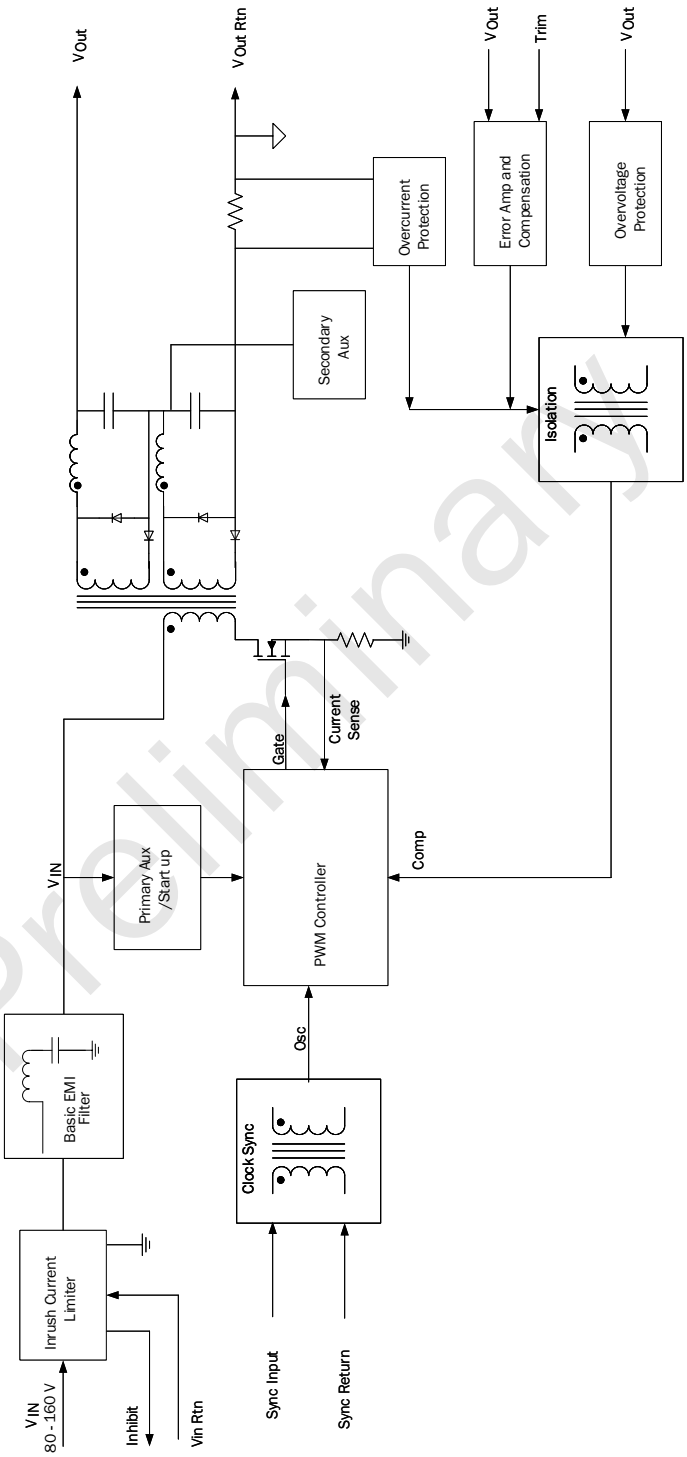

FIGURE 9: SMP120 BLOCK DIAGRAM 28 VOLT SINGLE

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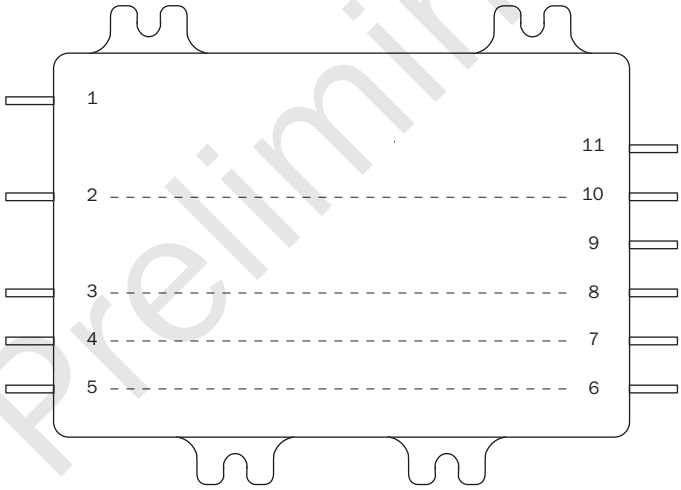
PIN OUT		
Pin	**5 Volt Single Output**	**28 Volt Single Output**
1	V_{IN}	V_{IN}
2	V_{IN} Return	V_{IN} Return
3	Inhibit	Inhibit
4	Sync (External Clock)	Sync (External Clock)
5	Sync Return	Sync Return
6	Trim	Trim
7	Sense Return	No Connection
8	V_{OUT} Return	V_{OUT} Return
9	V_{OUT}	V_{OUT}
10	Positive Sense	No Connection
11	Case	Case

TABLE 2: PIN OUT



For dimensions see Figure 42.

FIGURE 10: TOP VIEW PIN OUT

PINS NOT IN USE	
Inhibit	Leave unconnected
Sync In	Connect to Sync Return
Sense Lines	Must be connected to appropriate outputs
Trim	Leave unconnected
Case	Leave unconnected

FIGURE 11: PINS NOT IN USE

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MODEL NUMBERING KEY

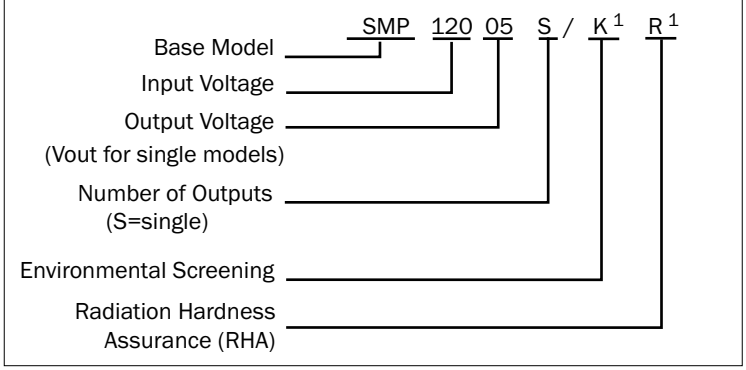

FIGURE 12: MODEL NUMBERING KEY

1. Screened to MIL-PRF-38534. Class H and K and RHA levels are pending product validation.

SMD NUMBERS	
STANDARD MICROCIRCUIT DRAWING (SMD)	**SMFL SERIES SIMILAR PART**
IN PROCESS 5962R1722301KXC	SMP12005S/KR
IN PROCESS 5962R1722302KXC	SMP12028S/KR
The SMD numbers shown are for RHA level R, screening level Class K, standard case (X), standard pin seal and non-solder dipped pins (C). For other options please refer to the SMD for the SMD number and the vendor similar number. All SMD numbers are listed on the SMD in the "Bulletin" which is the last page of the SMD. For exact specifications for an SMD product, refer to the SMD. SMDs can be downloaded from https://landandmaritimeapps.dla.mil/programs/smcr	

TABLE 3: SMD NUMBER CROSS REFERENCE

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MODEL NUMBER OPTIONS

TO DETERMINE THE MODEL NUMBER ENTER ONE OPTION FROM EACH CATEGORY IN THE FORM BELOW.

CATEGORY	Base Model and Input Voltage	Output Voltage	Number of Outputs [1]	Screening [2]	RHA [3]
OPTIONS	SMP120	05, 28	S	O H K	O P L R
FILL IN FOR MODEL # [4]	SMP120 _____	_____	_____	/ _____	_____

Notes
1. Number of Outputs: S is a single output.
2. Screening: Screened to MIL-PRF-38534. Class H and K are pending product validation. A screening level of O is a Space Prototype and is only used with RHA O. See Table 7 and Table 8 for more information.
3. RHA: Screened to MIL-PRF-38534. RHA R is pending product validation. Interpoint model numbers use an "O" in the RHA designator position to indicate the "-" (dash) RHA level of MIL-PRF-38534, which is defined as "no RHA." RHA O is only available with screening level O. See Table 8 for more information.
4. If ordering by model number add a "-Q" to request solder dipped leads (SMP12005S/KR-Q).

TABLE 4: MODEL NUMBER OPTIONS

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TABLE 5: OPERATING CONDITIONS - ALL MODELS, 25°C CASE, 120 VIN UNLESS OTHERWISE SPECIFIED.

		ALL MODELS			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LEAD SOLDERING TEMPERATURE [1]	10 SECONDS MAX.	—	—	300	°C
STORAGE TEMPERATURE [1]		-65	—	+150	°C
CASE OPERATING TEMPERATURE	SEE TABLE 5: ELECTRICAL CHARACTERISTICS				
ESD RATING [1, 2] MIL-PRF-38534, 3.9.5.8.2	MIL-STD-883 METHOD 3015 CLASS TBD, T_C = 25°C	—	—	TBD	V
ISOLATION: INPUT TO OUTPUT, INPUT TO CASE AND OUTPUT TO CASE [3]	@ 500 VDC, T_C = 25°C	100	—	—	Megohms
CAPACITANCE: INPUT TO OUTPUT		—	800	—	pF
UNDERVOLTAGE LOCKOUT [4] T_C = -55°C TO +125°C	RISING V_{IN} (TURN ON)	—	75	79.5	V
	FALLING V_{IN} (TURN OFF)	69	75	—	
CURRENT LIMIT [5] T_C = -55°C TO +125°C	% OF FULL LOAD	110	—	145	%
AUDIO REJECTION [1]	T_C = 25°C	—	50	—	dB
OUTPUT VOLTAGE TRIM RANGE T_C = -55°C TO +125°C	SEE PAGE 5	—	±10	—	%
	NOT USED	LEAVE PIN OPEN			
SWITCHING FREQUENCY T_C = -55°C TO +125°C	OPERATING FREQUENCY	450	500	535	kHz
SYNCHRONIZATION [6] T_C = -55°C TO +125°C	INPUT FREQUENCY	450	—	550	kHz
SYNC IS FLOATING AND ISOLATED T_C = -55°C TO +125°C	DUTY CYCLE	30	—	70	%
	ACTIVE LOW	—	—	0.8	V
	ACTIVE HIGH	3	—	5	
	REFERENCED TO	SYNC RETURN			
	IF NOT USED	CONNECT TO SYNC RETURN			
INHIBIT ACTIVE LOW (OUTPUT DISABLED) T_C = -55°C TO +125°C Do not apply a voltage to the inhibit pin	INHIBIT PIN PULLED LOW [1, 7]	—	—	1	V
	INHIBIT PIN SOURCE CURRENT [1]	—	—	500	µA
	REFERENCED TO	INPUT COMMON			
INHIBIT ACTIVE HIGH (OUTPUT ENABLED T_C = -55°C TO +125°C Do not apply a voltage to the inhibit pin	INHIBIT PIN CONDITION	OPEN COLLECTOR OR UNCONNECTED			
	OPEN INHIBIT PIN VOLTAGE [1]	10	12	13.6	V

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Notes
1. Characterization test and/or analysis. Not a production test.
2. Passes TBD volts.
3. When testing isolation, input pins are tied together and output pins are tied together. They are tested against each other and against case. Discharge the pins before and after testing.
4. Input voltage should rise and fall no slower than 50 volts/ms. If this is not possible, the SMP120 should be inhibited prior to the application or removal of power. See section on Sequencing on page 4.
5. Continuous operation at 125°C baseplate temperature, in an overload or full load, condition may result in permanent damage to the converter. During a near short-circuit load fault condition, when Vo falls to below ~2 volts, output will recover automatically when the fault current has been reduced to below 50% of rated full load.
6. Can only be synchronized above the default operating frequency.
7. Tested with Inhibit pin at <1.0 volts.

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TABLE 6: ELECTRICAL CHARACTERISTICS: -55°C TO +125°C CASE, 120 VIN, 100% LOAD, UNLESS OTHERWISE SPECIFIED.

SINGLE OUTPUT MODELS		SMP12005S			SMP12028S			UNITS
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE		4.90	5.00	5.10	27.4	28	28.6	V
OUTPUT CURRENT [2]	SEE DERATING FOOTNOTE	–	–	8.0	–	–	1.75	A
OUTPUT POWER [3]	SEE DERATING FOOTNOTE	–	–	40	–	–	49	W
CASE OPERATING	MAX TEMP AT FULL LOAD.	-55	–	110	-55	–	85	°C
TEMPERATURE [3]	MAX OPERATING TEMP	-55	–	125	-55	–	125	
OUTPUT RIPPLE	T_C = 25°C	–	50	100	–	25	85	mV p-p
20 Hz - 2 MHz	T_C = -55°C TO +125°C	–	–	100	–	–	85	
OUTPUT RIPPLE [4]	T_C = 25°C	–	50	175	–	50	125	mV p-p
20 Hz - 20 MHz	T_C = -55°C TO +125°C	–	–	175	–	–	125	
LINE REGULATION	V_{IN} = 80 TO 160 V	–	1	10	–	1	10	mV
LOAD REGULATION	NO LOAD TO FULL	–	1	10	–	25	140	mV
INPUT VOLTAGE	CONTINUOUS	80	120	160	80	120	160	V
	TRANSIENT 100 MS [1]	–	–	180	–	–	180	
INPUT CURRENT	NO LOAD	–	–	75	–	–	75	mA
	INHIBITED	–	–	1.2	–	–	1.2	
INPUT RIPPLE CURRENT	T_C = 25°C	–	20	65	–	25	65	mA p-p
20 HZ - 2 MHZ	T_C = -55°C TO +125°C	–	–	90	–	–	90	
INPUT RIPPLE CURRENT	T_C = 25°C	–	40	90	–	40	90	mA p-p
20 HZ - 20 MHZ	T_C = -55°C TO +125°C	–	–	90	–	–	90	
EFFICIENCY	T_C = 25°C	74	78	–	77	82	–	%
	T_C = -55°C to +125°C	74	–	–	75.5	–	–	
LOAD FAULT [5, 6]	POWER DISSIPATION	–	7	12	–	5	12	W
	RECOVERY	–	–	25	–	–	25	ms
STEP LOAD RESPONSE [6, 7, 8]	TRANSIENT	–	–	±350	–	–	±1000	mV pk
50% - 100% - 50%	RECOVERY	–		200	–	–	500	µs
STEP LINE RESPONSE [1, 6, 9]	TRANSIENT	–	±250	–	–	±1000	–	mV pk
V_{IN} = 80 - 160 - 80	RECOVERY	–	300	–	–	500	–	µs
START-UP [6, 10]	DELAY	–	–	25	–	–	25	ms
	OVERSHOOT	–	–	50	–	–	280	mV pk
CAPACITIVE LOAD [11, 12, 13, 14] T_C = 25°C	UNCONDITIONALLY STABLE, START-UP DELAY INCREASED	–	–	1000	–	–	200	µF

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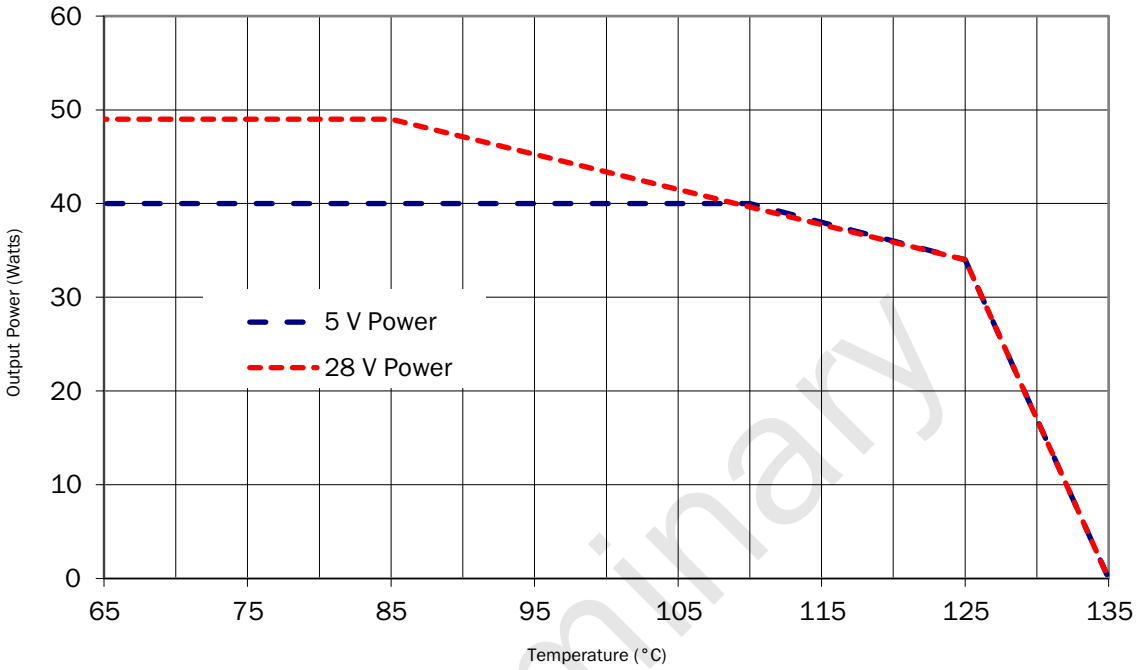
Notes
1. Characterization test and/or analysis. Not a production test.
2. 5 volt: Derate to 6.8 A at 125°C starting at 110°C.
   28 volt: Derate to 1.21 A at 125°C starting at 85°C.
3. 5 volt: Derate to 34 W at 125°C starting at 110°C.
   28 volt: Derate to 34 W at 125°C starting at 85°.
4. 20 MHz ripple measured with 0.01 µF capacitor connected as close as possible to V_{OUT} and V_{OUT} return pins.
5. Maximum power dissipation when output is shorted.
6. Recovery and start-up times are measured from application of the transient, or change in condition, to the point at which V_{OUT} is within 1% of final value.
7. Step load transition test is performed with load current rise time at 10 microseconds typical.
8. Half load to/from full load.
9. Step line test is performed with input voltage rise time at 100 microseconds ± 20 microseconds.
10. Measured from release of inhibit or input voltage step.
11. Minimum ESR: 0.05 ohms for 5 volt, 0.1 ohms for 28 volt.
12. Maximum ESR: 0.5 ohms for 5 volt, 1.0 ohms for 28 volt.
13. 5 volt - Up to 2.5% start up and short circuit recovery overshoot with capacitive loading.
14. 28 volt - Up to 8% start up and short circuit recovery overshoot with capacitive loading.

SMP120 Single Output Space DC-DC Converters

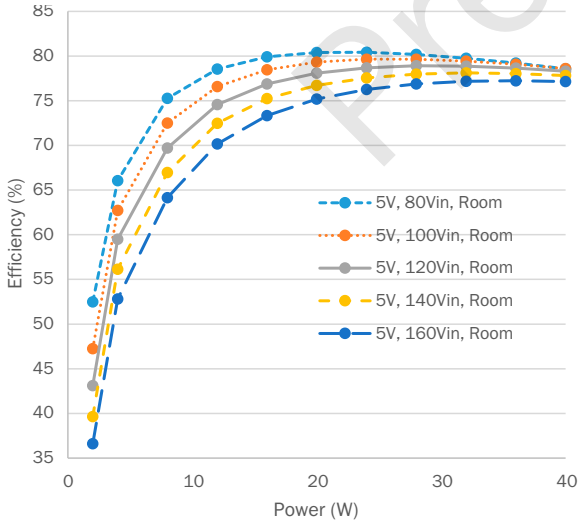
PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



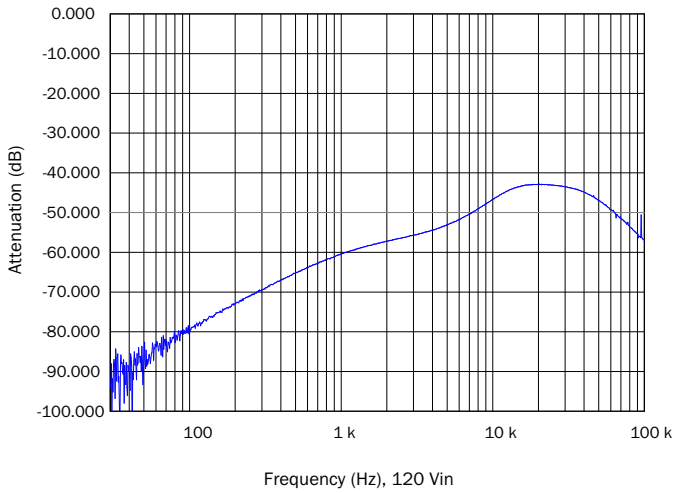
SMP12005S and SMP12028S Power Derating

FIGURE 13



SMP12005S Efficiency

FIGURE 14



SMP12005S Audio Rejection

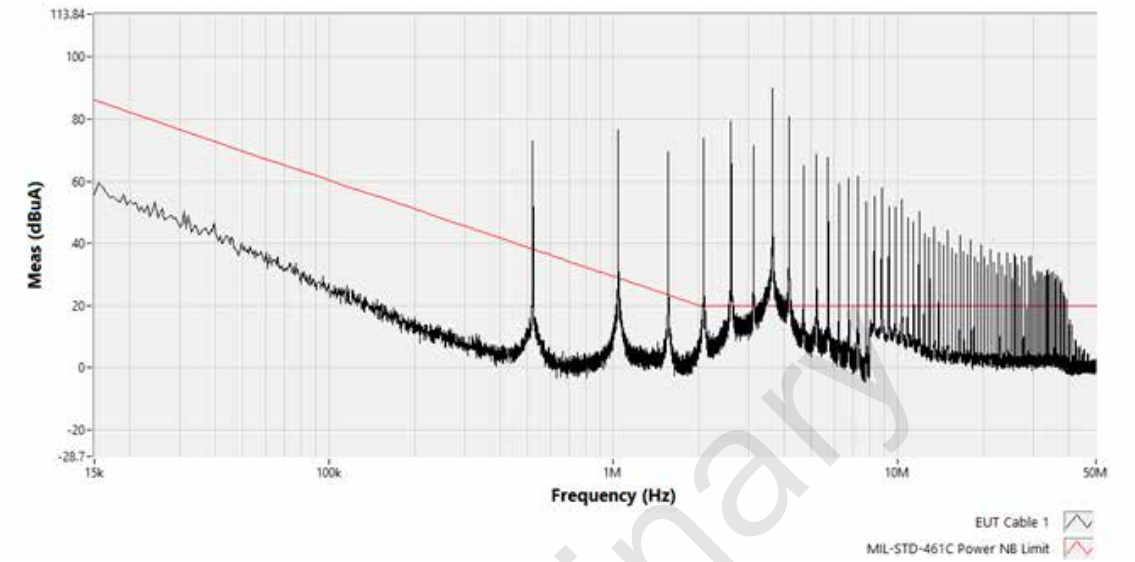
FIGURE 15

Preliminary

SMP120 Single Output Space DC-DC Converters

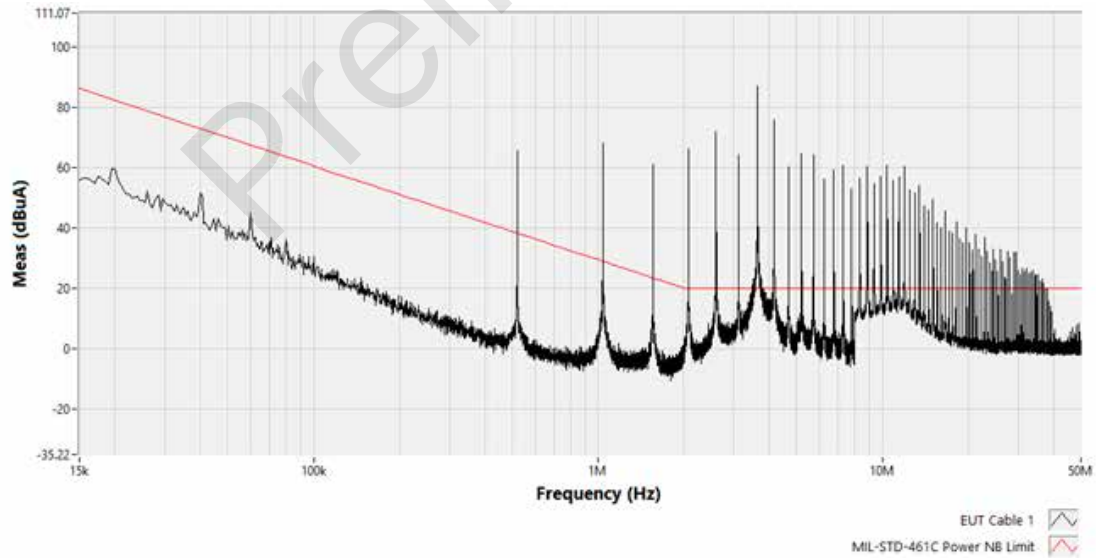
PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



SMP12005S, MIL-STD-461 CE03, Common Mode

FIGURE 16



SMP12005S, MIL-STD-461 CE03, Power Line

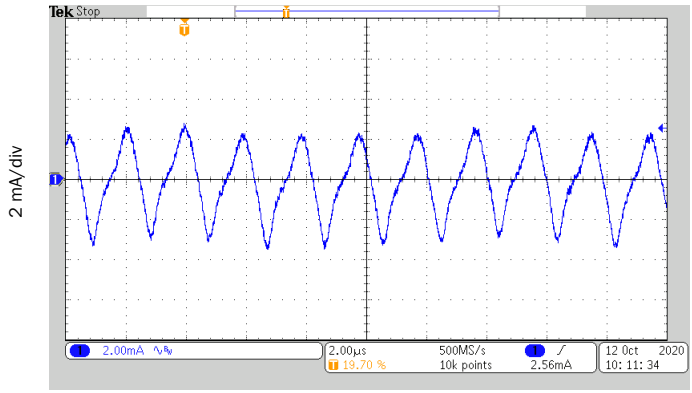
FIGURE 17

Preliminary

SMP120 Single Output Space DC-DC Converters

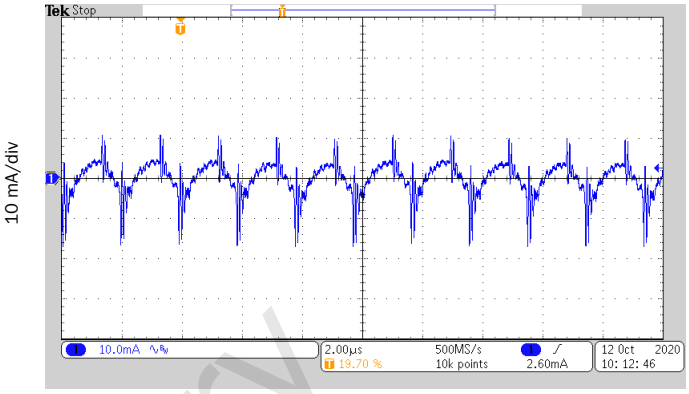
PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



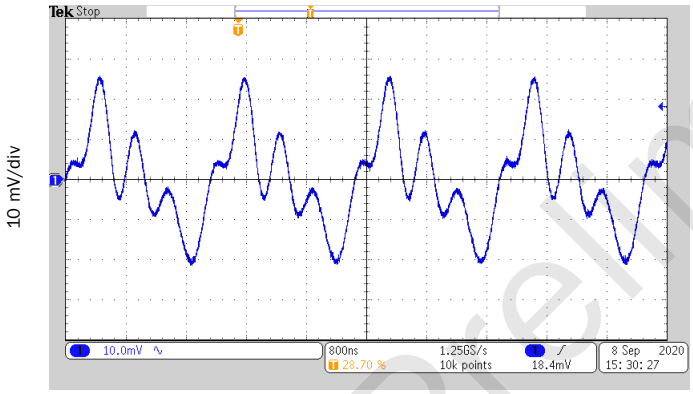
2 µs/div
SMP12005S I_{IN} Ripple - 2 MHz Bandwidth

FIGURE 18



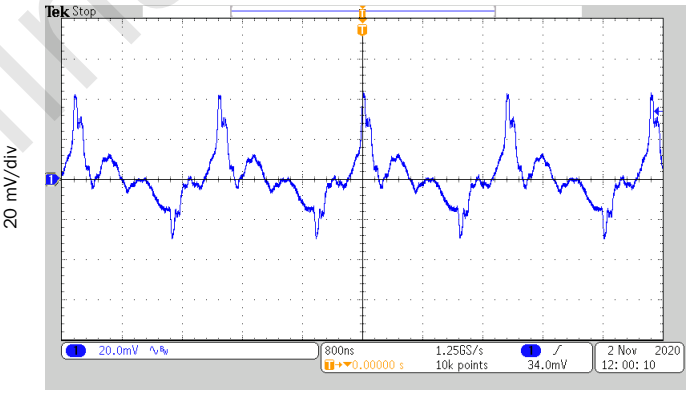
2 µs/div
SMP12005S I_{IN} Ripple - 20 MHz Bandwidth

FIGURE 19



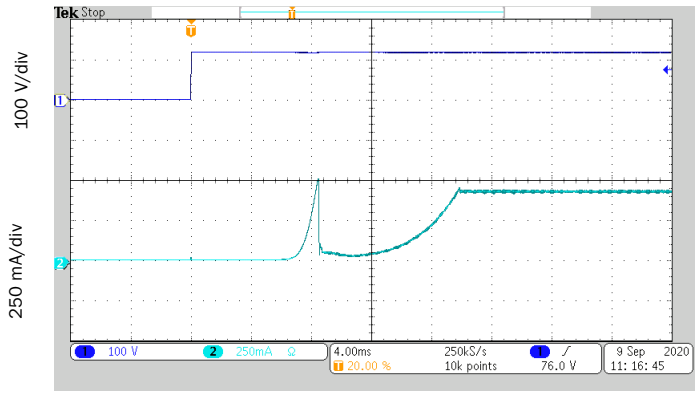
800 ns/div
SMP12005S Vout Ripple - 2 MHz Bandwidth

FIGURE 20



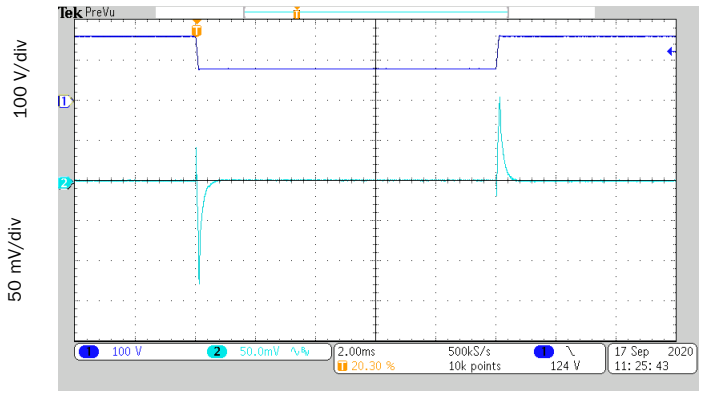
800 ns/div
SMP12005S Vout Ripple - 20 MHz Bandwidth

FIGURE 21



4 ms/div
SMP12005S Inrush Current

FIGURE 22



2 ms/div
SMP12005S Step Line

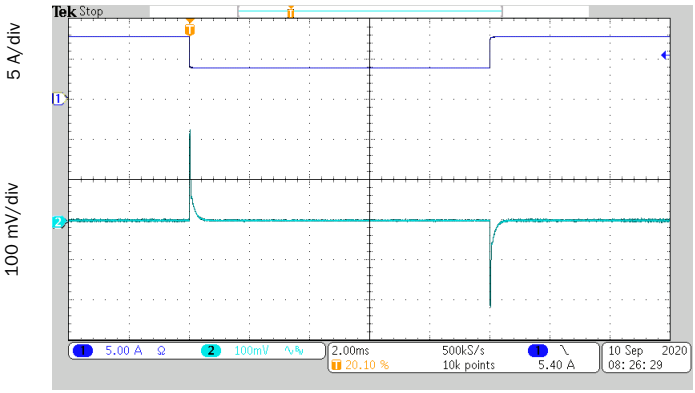
FIGURE 23

Preliminary

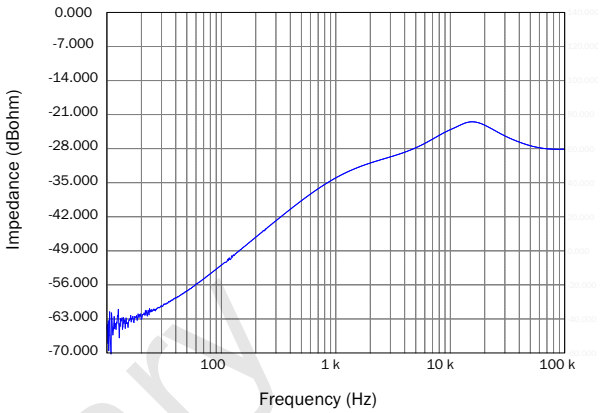
SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

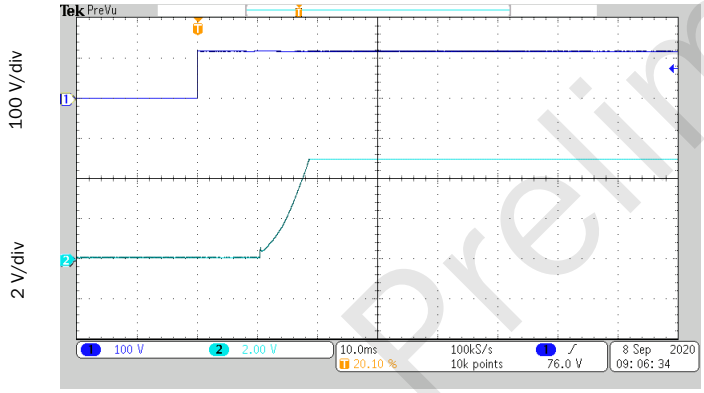
TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



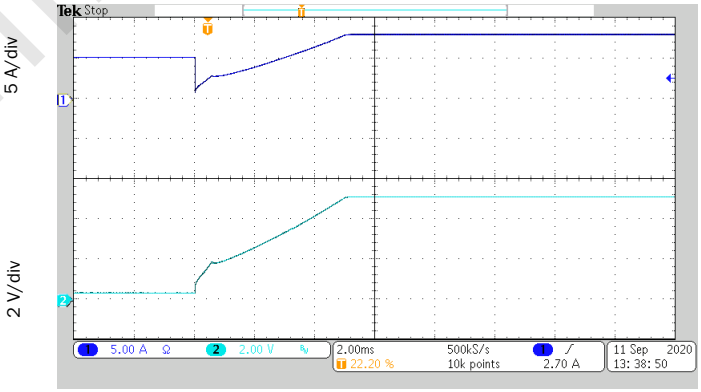
2 ms/div
SMP12005S Step Load
FIGURE 24



SMP12005S Output Z
FIGURE 25



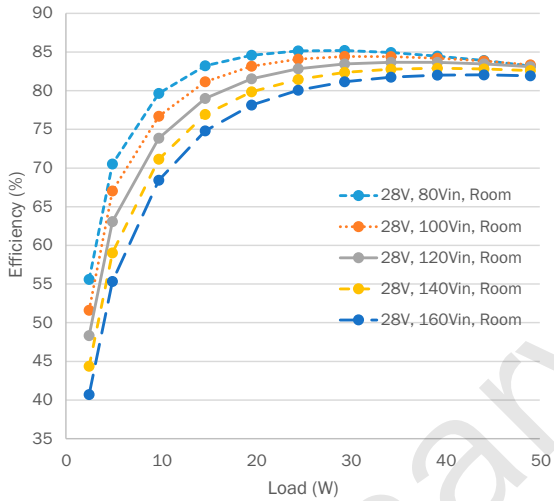
10 ms/div
SMP12005S Startup Overshoot
FIGURE 26



2 ms/div
SMP12005S Short Circuit Recovery
FIGURE 27

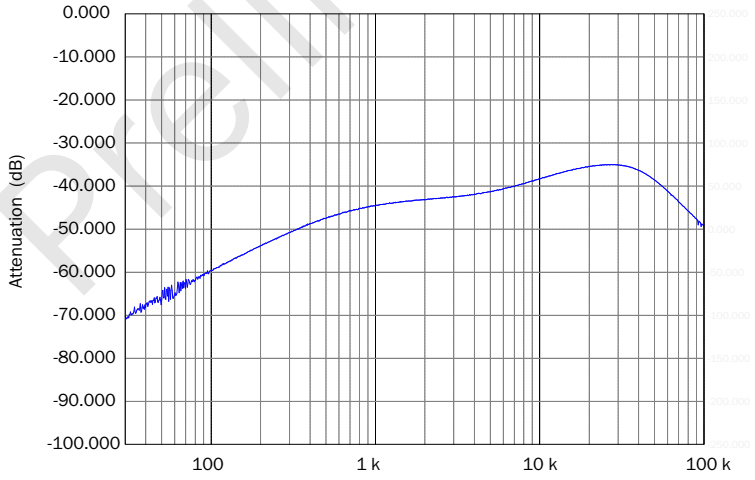
Preliminary

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



SMP120285S Efficiency

FIGURE 28

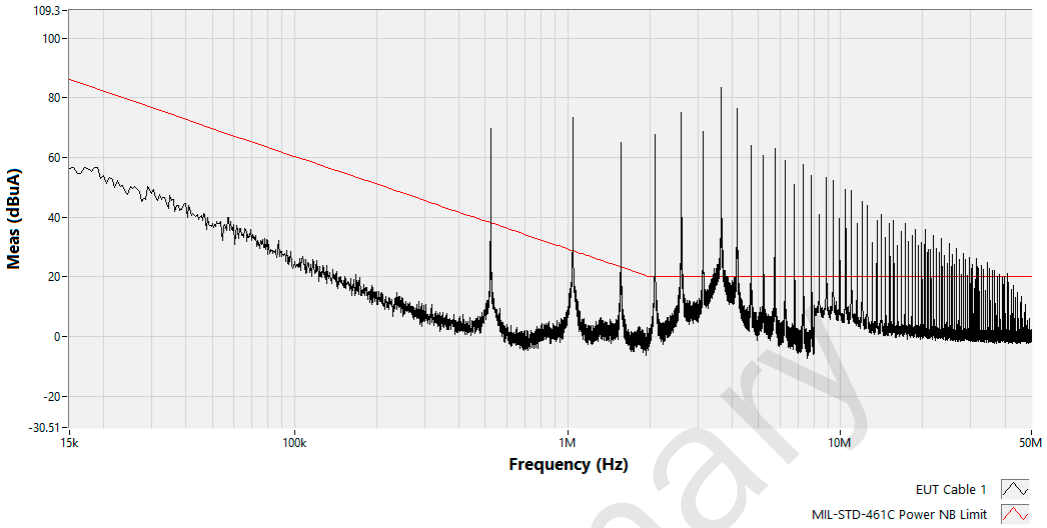


SMP12028S Audio Rejection

FIGURE 29

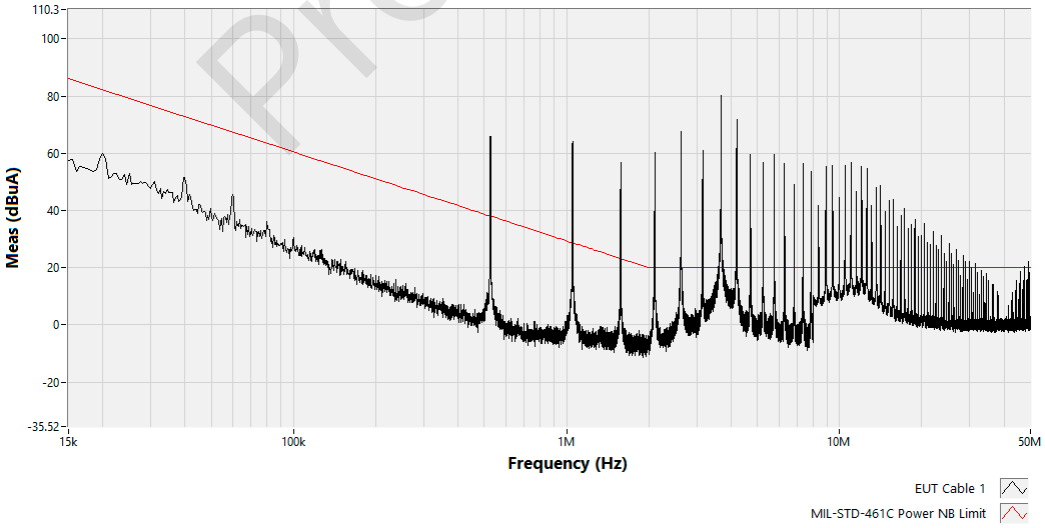
Preliminary

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



SMP12005S, MIL-STD-461 CE03, Common Mode

FIGURE 30



SMP12005S, MIL-STD-461 CE03, Power Line

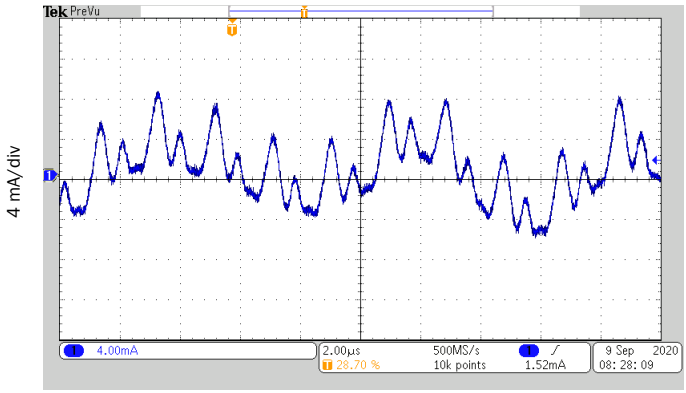
FIGURE 31

Preliminary

SMP120 Single Output Space DC-DC Converters

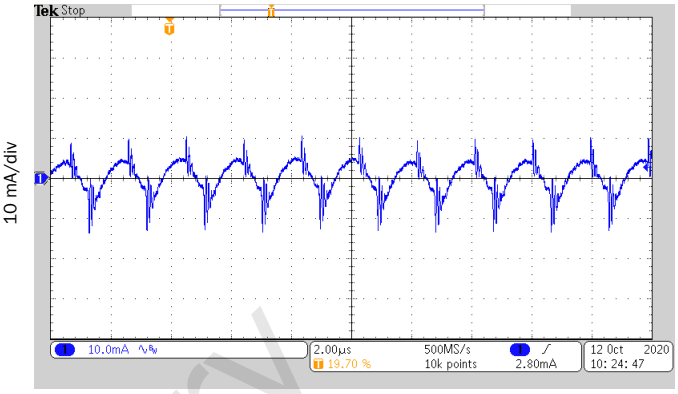
PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



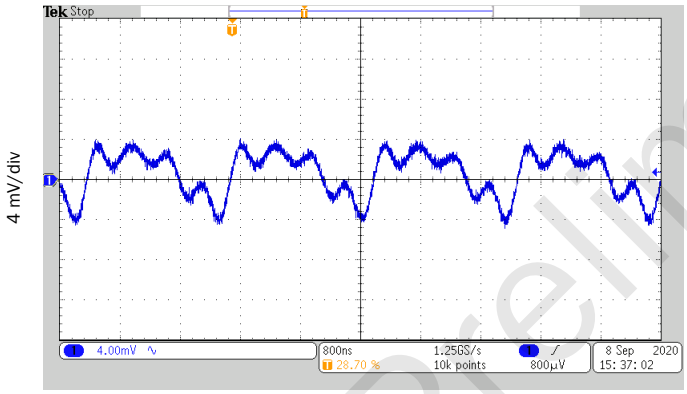
2 µs/div
SMP12028S I_{IN} Ripple - 2 MHz Bandwidth

FIGURE 32



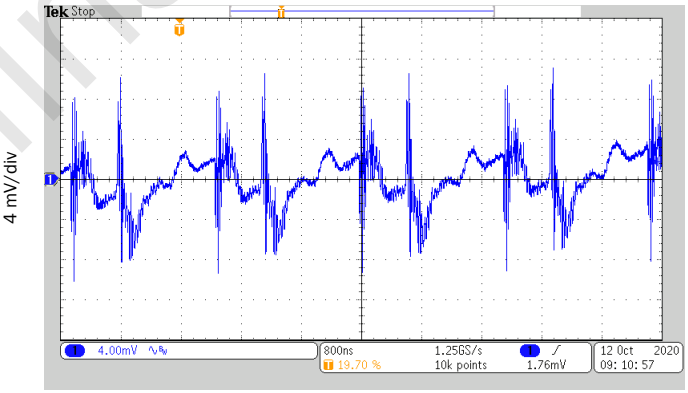
2 µs/div
SMP12028S I_{IN} Ripple - 20 MHz Bandwidth

FIGURE 33



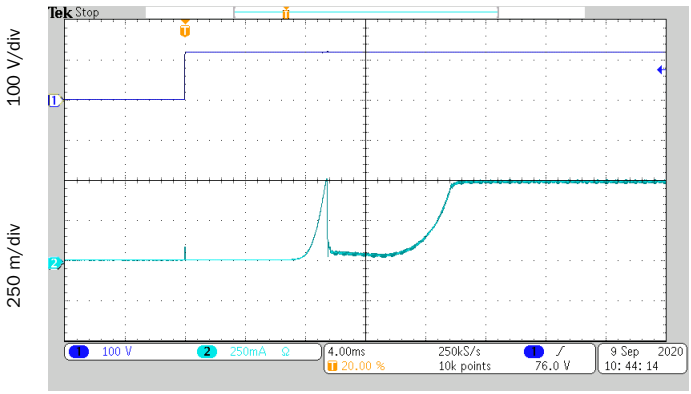
800 ns/div
SMP12028S Vout Ripple - 2 MHz Bandwidth

FIGURE 34



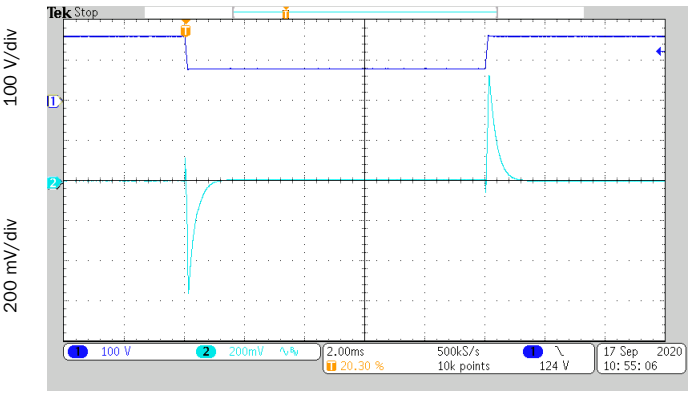
800 ns/div
SMP12028S Vout Ripple - 20 MHz Bandwidth

FIGURE 35



4 ms/div
SMP12028S Inrush Current

FIGURE 36



2 ms/div
SMP12028S Step Line

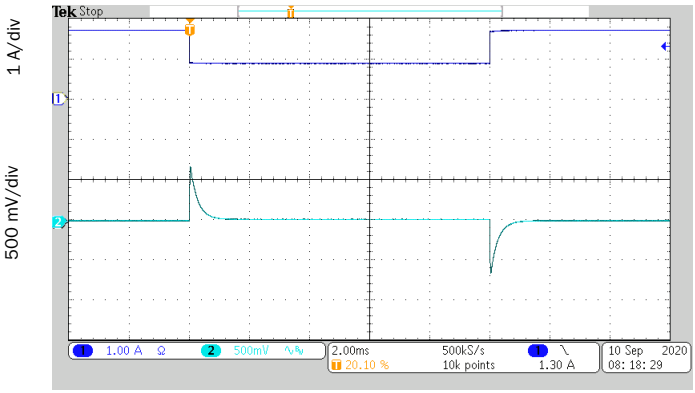
FIGURE 37

Preliminary

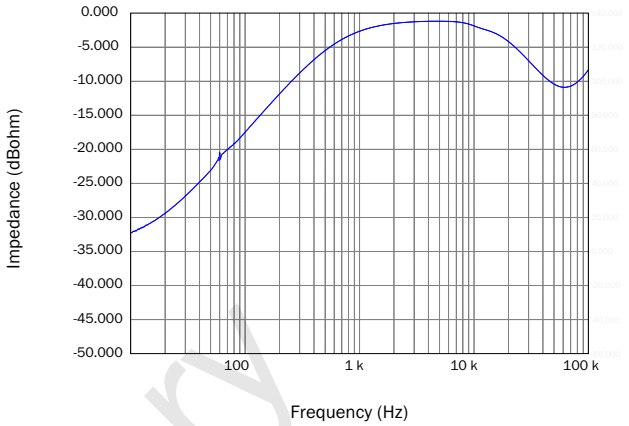
SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

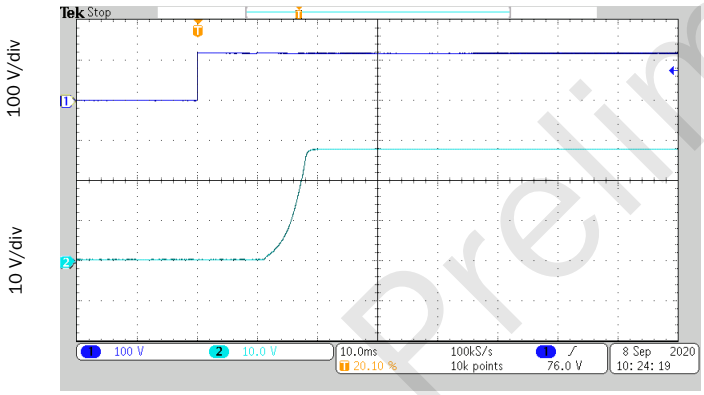
TYPICAL PERFORMANCE PLOTS: 25°C CASE, 120 VIN, 100% LOAD, FREE RUN, UNLESS OTHERWISE SPECIFIED.
THESE ARE EXAMPLES FOR REFERENCE ONLY AND ARE NOT GUARANTEED SPECIFICATIONS.



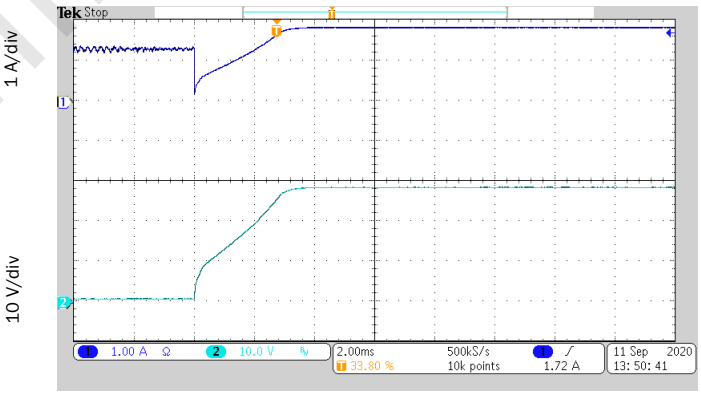
SMP12028S Step Load
FIGURE 38



SMP12028S Output Z
FIGURE 41



SMP12028S Startup Overshoot
FIGURE 39

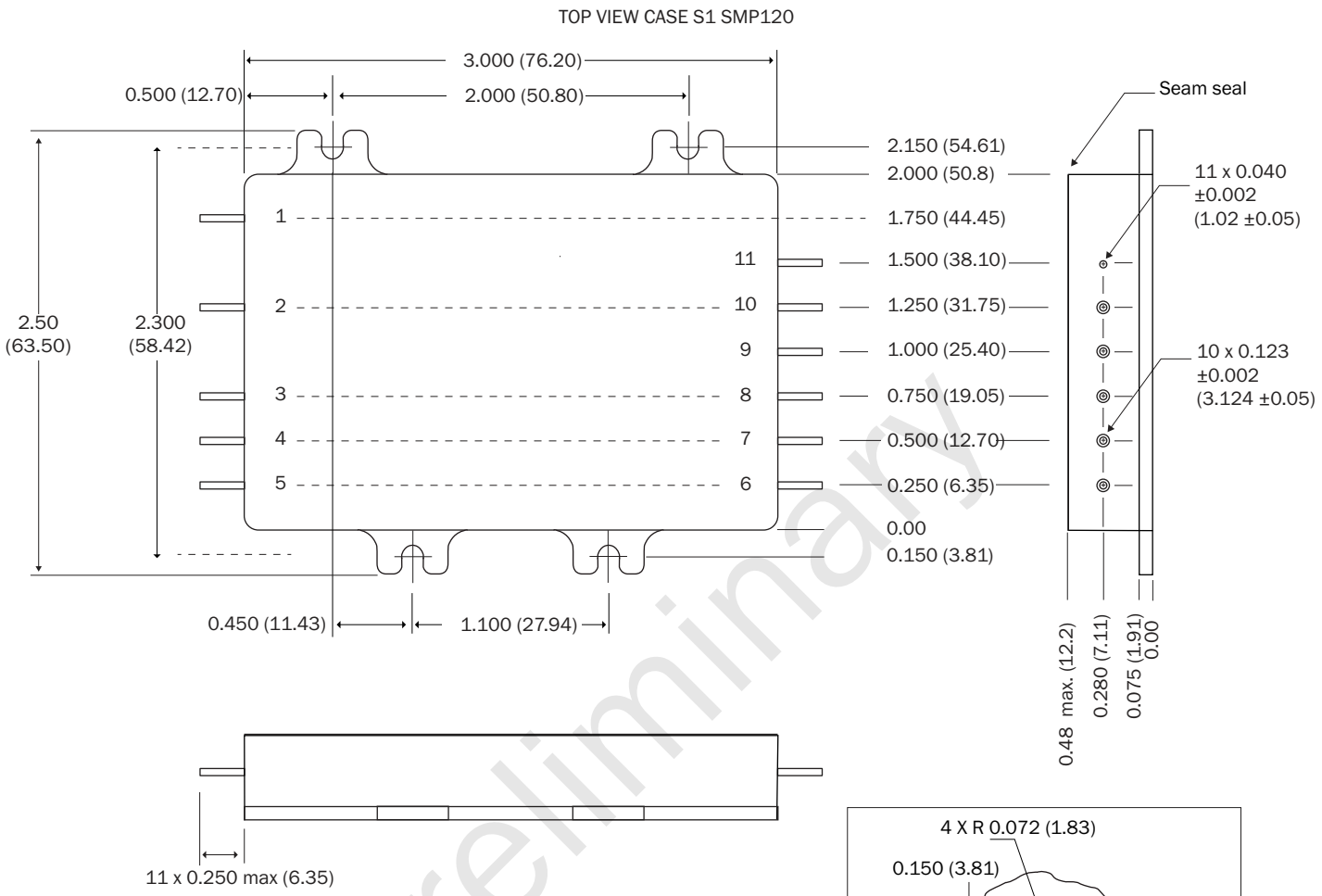


SMP12028S Short Circuit Recovery
FIGURE 40

Preliminary

SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS



Weight: 140 grams typical

Case dimensions in inches (mm)
Tolerance ±0.005 (0.13) for three decimal places
±0.01 (0.3) for two decimal places
unless otherwise specified

CAUTION
Heat from reflow or wave soldering may damage the device.
Solder pins individually with heat application not exceeding 300 °C for 10 seconds per pin

Materials
Header Cold Rolled Steel/Nickel/Gold
Cover Kovar/Nickel
Pins Copper cored 3:1 alloy 52, glass compression seal
Gold plating of 50 - 150 microinches included in pin diameter
Seal hole 0.091 ±0.002 (2.31 ±0.051)

Please refer to the numerical dimensions for accuracy.

FIGURE 42: CASE S1

Preliminary

SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

ELEMENT EVALUATION TABLES FOR QML PRODUCTS ARE IN "APP-009 QUALITY AND CERTIFICATION", APPENDIX A, IN COMPLIANCE WITH MIL-PRF-38534 REVISION L.
(LINK HTTPS://WWW.CRANEAE.COM/QUALITY-ASSURANCE-MODULAR-POWER)

ENVIRONMENTAL SCREENING SPACE DC-DC CONVERTERS PROTOTYPE, CLASS H AND K

	NON-QML [1]	QML [2, 3]	
TEST PERFORMED	**PROTOTYPE (/O) [4]**	**CLASS H (/H)**	**CLASS K (/K)**
Non-destruct wire bond pull, Method 2023		■ [5]	■
Pre-cap Inspection, Method 2017, 2032	■	■	■
Temperature Cycle (10 times)			
Method 1010, Cond. C, -65°C to +150°C, ambient	■	■	■
Constant Acceleration			
Method 2001, 3000 g	■	■	■
PIND, Test Method 2020, Cond. A		■ [5]	■
Pre burn-in test, Group A, Subgroups 1 and 4	■	■ [5]	■
Burn-in Method 1015, +125°C case, typical [6]			
96 hours	■		
160 hours		■	
2 x 160 hours (includes mid-BI test)			■
Final Electrical Test, MIL-PRF-38534, Group A,			
Subgroups 1 and 4: +25°C case	■		
Subgroups 1 through 6, -55°C, +25°C, +125°C case		■	■
Hermeticity Test, Method 1014			
Gross Leak, Cond. B_2, Kr85			■
Gross Leak, Cond. C_1, fluorocarbon	■	■	
Fine Leak, Cond. B_1, Kr85			■
Fine Leak, Cond. A_2, helium	■	■	
Radiography, Method 2012			■
Post Radiography Electrical Test, +25°C case			■ [5]
Final visual inspection			
Method 2009 of MIL-STD-883		■	■
Magnification 1X [7]	■		

Test methods are referenced to MIL-STD-883 as determined by MIL-PRF-38534.

Notes
1. Non-QML prototype products may not meet all of the requirements of MIL-PRF-38534.
2. All processes are QML qualified and performed by certified operators.
3. Class H or K QML products that have no SMD number are marked "CHP, CHL, CHR, CKP, CKL or CKR" per MIL-PRF-38534, Table III instead of "QML".
4. "O" in the RHA designator position in Interpoint model numbers indicates DLA RHA "-" defined as no RHA.
5. Not required by DLA but performed to assure product quality.
6. Burn-in temperature designed to bring the case temperature to +125°C minimum. Burn-in is a powered test.
7. Visual inspection is performed per an internal document. Product may contain cosmetic irregularities such as dents, dings, scratches, etc. that do not affect form, fit or function.

TABLE 7: ENVIRONMENTAL SCREENING SPACE DC-DC CONVERTERS PROTOTYPE, CLASS H AND K

Preliminary

SMP120 Single Output Space DC-DC Converters

PRELIMINARY – 80 TO 160 VOLT INPUT – 40 TO 49 WATTS

Space Radiation Hardness Assurance DC-DC Converters Class H and K, RHA [1] P, L and R

	QML [2]					
	Class H			Class K		
Qualification Per MIL-STD	/HP	/HL	/HR	/KP	/KL	/KR
RHA P: 30 krad(Si) total dose [3, 4]	■			■		
RHA L: 50 krad(Si) total dose [3, 4]		■			■	
RHA R: 100 krad(Si) total dose [3, 4]			■			■
SEE, LET 43 MeV cm^2/mg [5]	■	■	■	■	■	■

Test methods are referenced to MIL-STD-883 as determined by MIL-PRF-38534.

Notes

1. DLA has approved the RHA plan for Interpoint power products. Our SMD products with RHA "P", "L" or "R" code meet DLA requirements.
2. Class H or K QML products that have no SMD number are marked "CHP, CHL, CHR, CKP, CKL or CKR" per MIL-PRF-38534, Table III instead of "QML".
3. Radiation sensitive components internal to the devices are procured with radiation guarantees or undergo radiation lot acceptance testing (RLAT) performed per condition A, method 1019 of MIL-STD-883.
4. Representative devices were initially High Dose Rate (HDR) tested using condition A of method 1019 of MIL-STD 883 to ensure RHA designator levels. Representative devices have also been Low Dose Rate (LDR) tested using condition D of method 1019 of MIL-STD-883 to the RHA designator levels. Representative devices will also be re-tested after design or process changes that can affect RHA response of this device.
5. Single event testing was performed on a converter to 43 MeV-cm^2/mg using 15 MeV/nucleon gold ions with no latch-up, burn-out, functional interrupts, or gate ruptures exhibited. Single event upsets (output voltage transients) may be present up to 43 MeV-cm^2/mg.

Table 8: Space Radiation Hardness Assurance DC-DC Converters Class H and K, RHA P, L and R

Preliminary